



Contents

Acknowledgements	i
Abstract (English/Français/Ελληνικά)	iii
List of figures	xlii
List of tables	xix
Symbols	xxi
Acronyms and Abbreviations	xxv
1 Introduction	1
1.1 Motivation	1
1.2 The MOS Transistor	2
1.3 Compact and Analytical Modeling	4
1.4 State-of-the-Art	8
1.4.1 Compact Modeling	8
1.4.2 Analytical RF MOSFET modeling	11
2 Technology, DUT and Measurements Description	13
2.1 Introduction	13
2.2 Technology Details	13
2.3 DUT Details	15
2.4 Measurement Details	16
I Analytical Small-Signal RF Modeling	19
3 Analytical RF Modeling	21
3.1 Introduction	21
3.2 MOSFET Equivalent Circuit at RF	22
3.3 Y-parameters Analysis	24
3.4 Expressions for the Direct Extraction of the RF Components	26
3.5 Parameter Extraction from Measurements	27
	ix

3.5.1	Validation of the Analytical RF Model	31
3.6	RF Figures-of-Merit	31
3.6.1	Current Gain - H_{21}	31
3.6.2	Transit Frequency - F_t	37
3.6.3	Unilateral Gain - U	39
3.6.4	Maximum Oscillation Frequency - F_{max}	43
3.7	Conclusions	43
4	Analytical RF Noise Modeling	47
4.1	Introduction	47
4.2	RF Noise Analysis	48
4.2.1	Step-by-step Derivation of the Analytical Expressions of the Four RF Noise Parameters	50
4.3	Expressions for the Direct Extraction of the RF Noise Model Parameters	59
4.3.1	Validation of the Analytical RF Noise Model and the Parameter Extraction Procedure	60
4.4	Conclusions	63
II	Compact Modeling with BSIM6	67
5	The BSIM6 Compact Model	69
5.1	Introduction	69
5.2	A Short History	69
5.3	BSIM6 Main Characteristics	70
6	Geometrical Scaling in BSIM6	73
6.1	Introduction	73
6.2	Geometrical Scaling Approaches	73
6.2.1	Comparison of Existing Geometrical Scaling Approaches	75
6.3	Selection of Geometrical Scaling Equations for BSIM6	77
6.4	Evaluation of the BSIM6 Scalability	82
6.5	Conclusions	84
7	Parameter Extraction Methodology of BSIM6 for CMOS Technologies	89
7.1	Introduction	89
7.2	Parameter Extraction Methodology	90
7.2.1	Extraction of Main Physical Effects & Geometry Independent Parameters	91
7.2.2	Extraction of Short Channel Effects & Length Scaling Parameters	95
7.2.3	Extraction of Narrow Channel Effects & Width Scaling Parameters	99
7.2.4	Extraction of Parameters for Narrow/Short Channel Devices	101
7.2.5	Extraction of Temperature Dependence Parameters	103
7.3	Conclusions	106

8	Evaluation of BSIM6 in Nanoscale CMOS Technologies	109
8.1	Introduction	109
8.2	Validation against a 40 nm CMOS Process	110
8.2.1	CV Operation	110
8.2.2	DC Operation	111
8.2.3	RF Operation	115
8.3	Validation against a 28 nm CMOS Process	125
8.3.1	CV Operation	126
8.3.2	DC Operation	130
8.4	Conclusions	130
III	Analytical Modeling of FoMs	135
9	Device Level Figures-of-Merit as Design Guidelines	137
9.1	Introduction	137
9.2	Modeling the Gate Transconductance - G_m	138
9.2.1	Modeling the Normalized Source Transconductance - g_{ms}	138
9.2.2	Extraction of Parameters - n , I_{spec} , λ_c	140
9.2.3	Model Verification	144
9.3	Modeling the Transconductance Efficiency - G_m/I_D	147
9.4	Modeling the Output Conductance - G_{ds}	150
9.4.1	Extraction of Parameters - α_{dibl} , λ_{sat_gds}	151
9.4.2	Model Verification	155
9.5	Modeling the Intrinsic Voltage Gain - A_{vi}	155
9.6	Modeling the Transit Frequency - F_t	159
9.6.1	Extraction of Parameters - C_{GGew}	160
9.6.2	Model Verification	161
9.7	Modeling the $G_m/I_D \cdot F_t$ RF FoM	161
9.8	Modeling the Noise Factor - F	164
9.8.1	Extraction of Parameters - R_G , γ_{nd}	167
9.8.2	Model Verification	168
9.9	Single-Transistor Common-Source Amplifier	169
9.10	Conclusions	175
10	Conclusion	177
10.1	Summary of Results	178
10.1.1	Analytical Small-Signal RF Modeling	178
10.1.2	Compact Modeling with BSIM6	178
10.1.3	Analytical Modeling of FoMs	179
10.1.4	General Remark	179
10.2	Suggestions for Future Work	180

Contents

Bibliography	183
Curriculum Vitae	195