

Contents

Acknowledgements	i
Abstract (English/Français)	iii
Table of Contents	ix
List of Figures	xi
List of Tables	xvii
1 Introduction	1
1.1 Operation at a Different Temperature	1
1.1.1 Heating or Self-Heating?	2
1.1.2 Observing Self-Heating Effects	3
1.1.3 Why a Single Device?	5
1.1.4 Self-Heating Related Issues	6
1.1.5 Scope of This Work	7
1.2 State of the Art	7
1.3 Key Contributions of This Thesis	10
1.4 Thesis Outline	11
2 Device Level Analysis of Self-Heating	13
2.1 Introduction	13
2.2 Theoretical Background and Related Work	14
2.2.1 Block Level Thermal Simulations	14
2.2.2 Device Level Thermal Simulations	15
2.3 Details of Our Device Level Simulations	17
2.4 Comparison of FDSOI and Bulk	19
2.4.1 Physical Structure and Thermal Boundary Conditions	19
2.4.2 Results and Discussions	21
2.5 Experiments on FDSOI	25
2.5.1 Effect of Drain Voltage	25
2.5.2 Effect of Gate Voltage	27
2.5.3 Effect of Gate Length	29
2.5.4 Effect of BOX Thickness	31

2.5.5	Effect of Drain and Source Contact Thermal Resistance	31
2.6	Conclusion	32
3	Thermal Aware Design of High Performance Digital Circuits	33
3.1	Introduction	33
3.2	Method for Block Level Thermal Simulations	35
3.2.1	Creation of Heat Maps	36
3.2.2	Thermal Model	37
3.2.3	Creation of Temperature Maps	39
3.3	Design of 64-bit Parallel Prefix Adders for Thermal Analysis	39
3.3.1	Architecture	40
3.3.2	Performance	45
3.4	Comparison of Bulk and FDSOI in 40 nm and 28 nm Nodes	47
3.4.1	Heating	47
3.4.2	Temperature	51
3.4.3	Simulation Time	64
3.5	Circuit Level Analysis of Hot-Spots	65
3.5.1	Heat Density of Individual Devices	65
3.5.2	Self-Heating of Devices with Different Functions	67
3.6	Conclusion	72
4	Self-Heating Effects on the Noise Performance of FDSOI MOSFETs	73
4.1	Introduction	73
4.2	Thermal Noise	74
4.2.1	Theoretical Background and Related Work	75
4.2.2	Thermal Noise Considering Self-Heating	76
4.3	Flicker Noise	82
4.3.1	Theoretical Background and Related Work	82
4.3.2	Flicker Noise Considering Self-Heating	84
4.4	Conclusion	85
5	Self-Heating Aware Design of LNAs with Short Channel Devices	87
5.1	Integrated Inductor Design	87
5.1.1	Undesired Effects	88
5.1.2	Lumped Model of an Integrated Inductor	89
5.1.3	Parametric Cell (pCell) for Integrated Inductors	94
5.2	Common Gate Cascode LNA	99
5.2.1	Design Parameters	99
5.2.2	Optimum Bias Point for Lowest Noise Figure	110
5.3	Measurements	115
5.3.1	Results	117
5.3.2	Comments	120
5.4	Conclusion	120

6	Flicker Noise Measurements	121
6.1	Test Blocks	121
6.1.1	Practical Considerations	123
6.1.2	Input Referred Noise	126
6.2	Measurement Results	128
6.2.1	Measurement Procedure	130
6.2.2	Results of Experiment-A	136
6.2.3	Results of Experiment-B	139
6.3	Conclusion	142
7	Conclusion	143
	Bibliography	156
	Curriculum Vitae	